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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,152	03/29/2004	Ga Won Lee	123034-05004767	8475

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EXAMINER	
GURLEY, LYNNE ANN	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/811,152	LEE, GA WON
	Examiner	Art Unit
	Lynne A. Gurley	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,4,7 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,4,7 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/028,972.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the preliminary amendment filed 3/29/04.

Currently, claims 3-4 and 7-8 are pending.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file 10/028,972.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 3/29/04 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the steps of removing the conductive material at a removal region and burying an interlayer dielectric film between the pattern at the removal region as described in the specification. Perhaps there should be a conductive layer 78 filled in between the 2nd and 3rd conductive lines in figure 6A and the removal step should be shown in figure 6B. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should

include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the drawings. Applicant's thorough review of the drawings is requested (especially in coordination with the specification).

Specification

4. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are: page 1, lines 23-24, "(intermetal dielectric is deposition)"; on page 2, lines 11-12, "a method

by an insulating spacer (wordline spacer or bitline spacer) is formed"; on page 10, regarding figure 6B, the removal of the insulator between the bitlines 75 is not explained.

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Grewal et al. (US 5,723,381, dated 3/3/98).

3. Grewal shows the method as claimed in figures 1B-1F as: forming conductive layer patterns (bitlines 1/ 2) and an insulating film spacer 3 on a sidewall of the conductive layer patterns through a common process; burying a conductive material 4 between the conductive layer patterns; removing the conductive material at a removal region (fig 1D) such that the conductive material remains at remaining regions to form a contact plug 4 (fig. 1E); and burying an interlayer dielectric film 6 between the conductive layer patterns at the removal region.

4. Claims 7-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Park et al. (US 6,753,252, dated 6/22/04, filed 5/18/01).

5. Park shows the method as claimed in figures 1,3-5, and 7-8 as: forming conductive layer patterns (bitlines or wordlines 12) and an insulating film spacer 26 (fig. 1) on a sidewall of the conductive layer patterns through a common process; burying a conductive material 42 between the conductive layer patterns; removing the conductive material at a removal region (fig 7) such that the conductive material remains at remaining regions to form a contact plug 50 (fig. 7-8); and burying an interlayer dielectric film 52 between the conductive layer patterns at the removal region.

6. Claims 3-4 and 7-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Park et al. (US 6,387,759, dated 5/14/02, filed 4/27/99).

7. Park shows the method as claimed in figures 9A-9E as: forming a conductive layer (bitlines or wordlines 206) pattern and an insulating film spacer 212/224 on a sidewall of the conductive layer pattern through a common process; removing the insulating film spacer in a region other than a contact plug formation region (fig. 9D right side of figure); and forming an interlayer dielectric film on an entire surface of the semiconductor device (fig. 9E).

Park also shows the method as claimed in figures 7A-7D, and 9A-E as: forming conductive layer patterns (bitlines or wordlines 206) and an insulating film spacer 212 (fig. 7B) on a sidewall of the conductive layer patterns through a common process; burying a conductive material 214 between the conductive layer patterns; removing the conductive material at a removal region (fig 7C-7D) such that the conductive material remains at remaining regions to

form a contact plug 216/218 (fig. 7D); and burying an interlayer dielectric film 219 (fig. 7D) between the conductive layer patterns at the removal region.

8. Claim 3 is rejected under 35 U.S.C. 102(e) as being anticipated by Lee (US 6,228,756, dated 5/8/01, filed 8/10/99).

9. Lee shows the method as claimed in figures 1A-1D and corresponding text, as: forming a conductive layer 102 pattern and an insulating film spacer 104/106 on a sidewall of the conductive layer pattern through a common process; removing the insulating film spacer in a region other than a contact plug formation region (fig. 1C, 106); and forming an interlayer dielectric film 110 on an entire surface of the semiconductor device (fig. 1D).

Claim 3 is rejected under 35 U.S.C. 102(e) as being anticipated by Jin et al. (US 6,350,665, dated 2/26/02, filed 4/28/00).

10. Jin shows the method as claimed in figures 1-6 and corresponding text, as: forming a conductive layer (204/206 or 404/406) pattern and an insulating film spacer (208/210 in fig. 2A or 410/408) on a sidewall of the conductive layer pattern through a common process; removing the insulating film spacer (210 or 410 in fig. 4) in a region other than a contact plug formation region (fig. 4C); and forming an interlayer dielectric film on an entire surface of the semiconductor device (fig. 4D-4F).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See the PTO Form 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is 571-272-1670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lynne A. Gurley
Primary Patent Examiner
Art Unit 2812

LAG
February 1, 2006